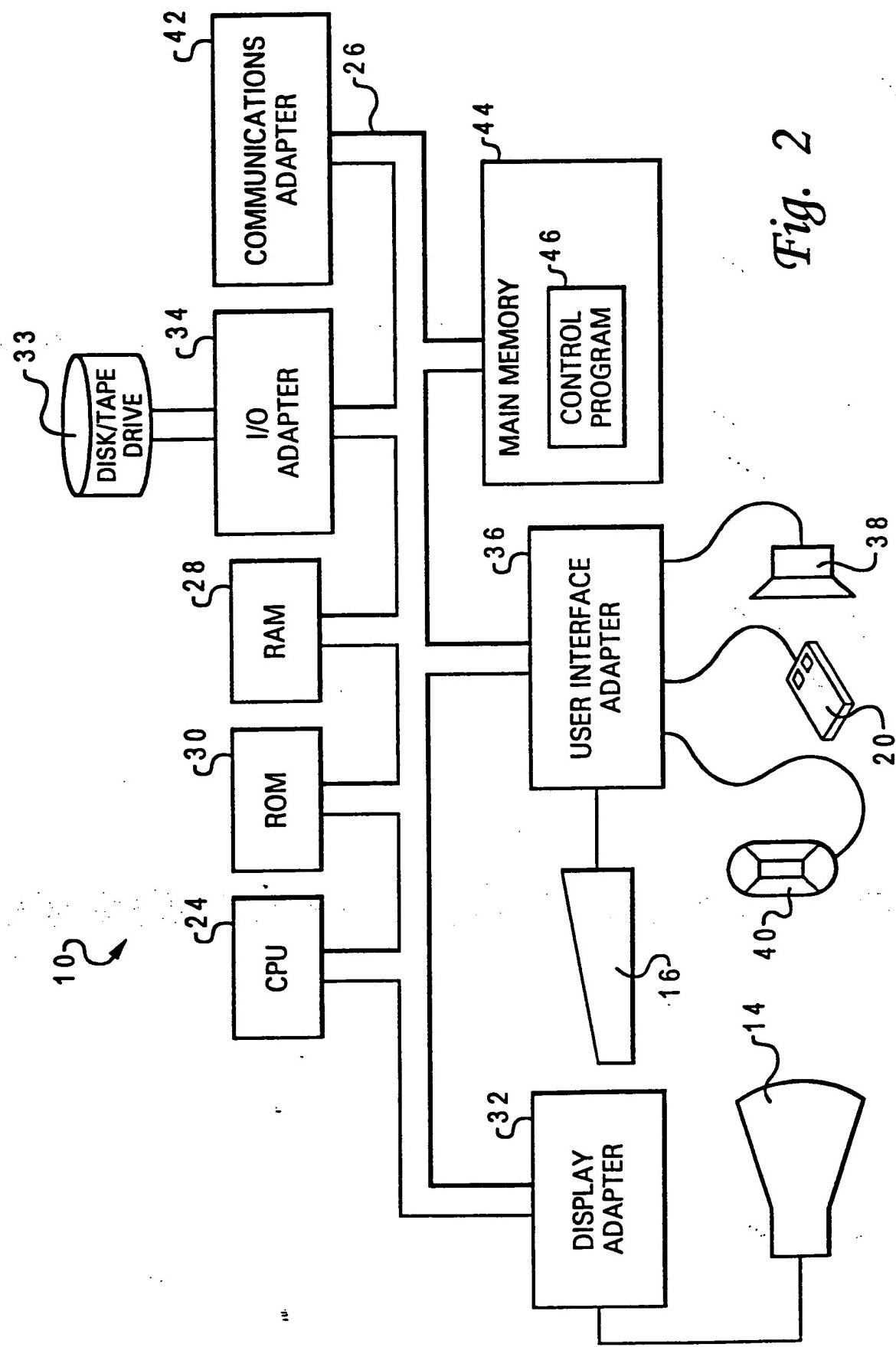


Fig. 1

Fig. 2



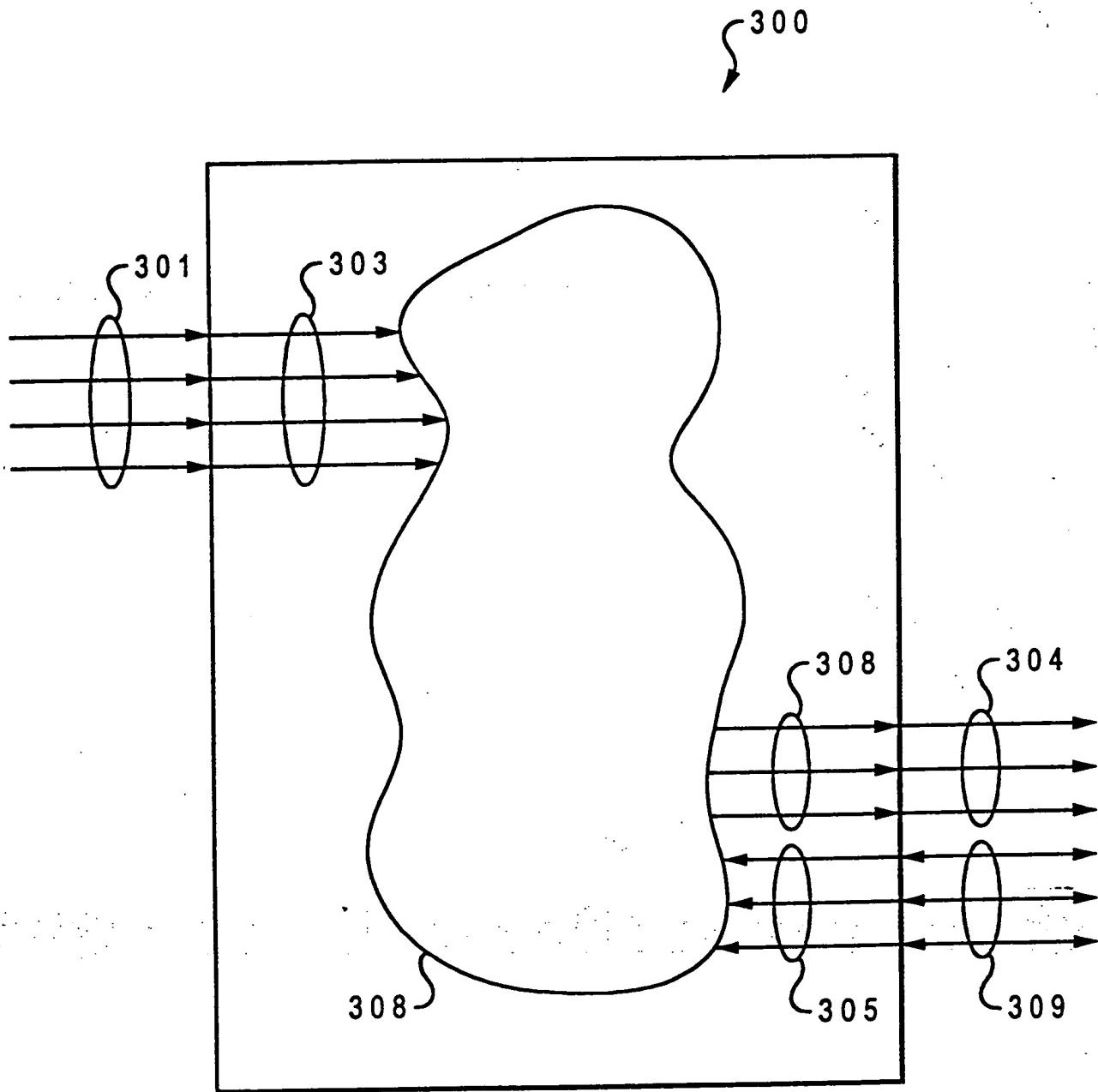


Fig. 3A

000E21F "FIGURE 3B

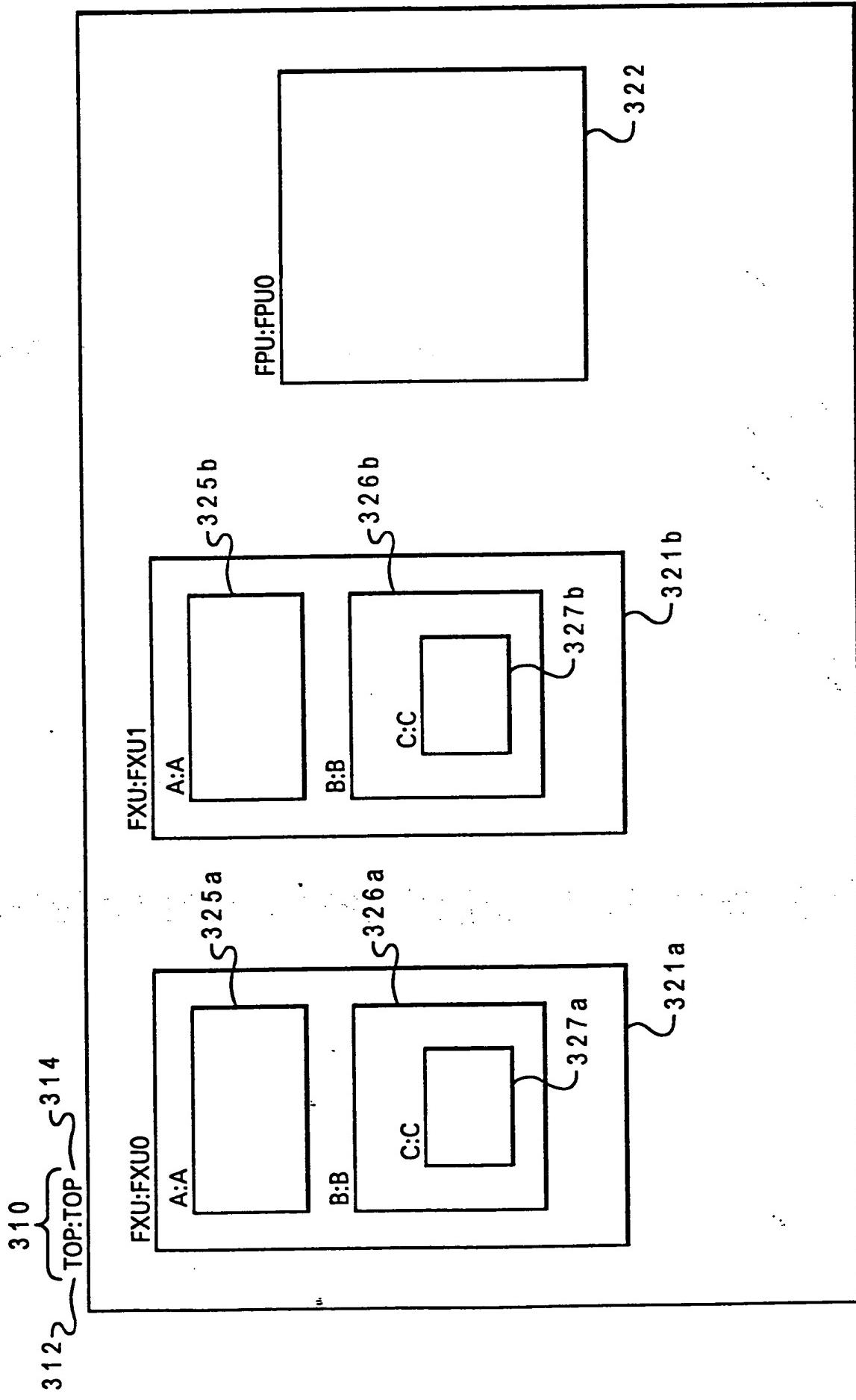


Fig. 3B

329 }

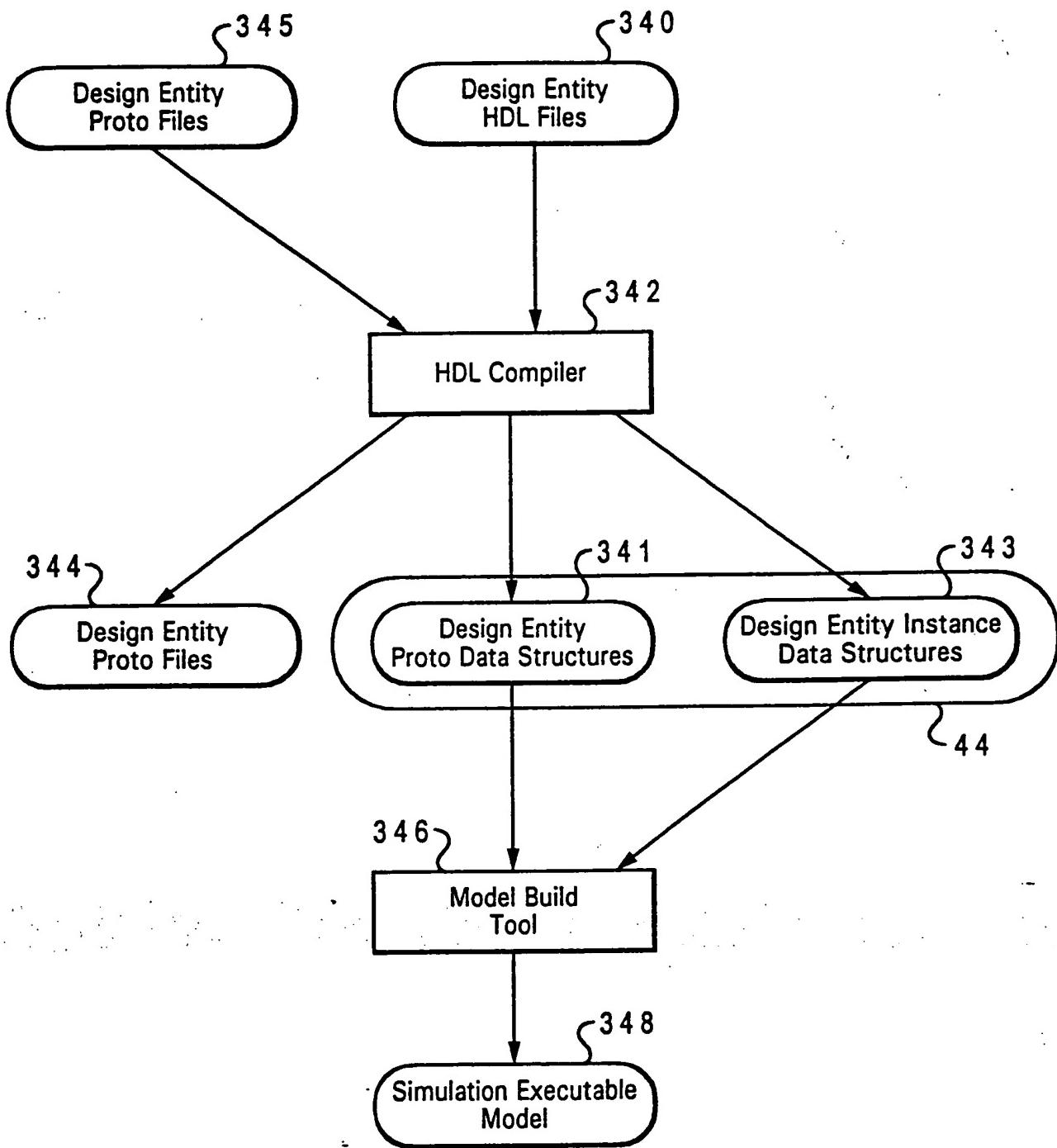
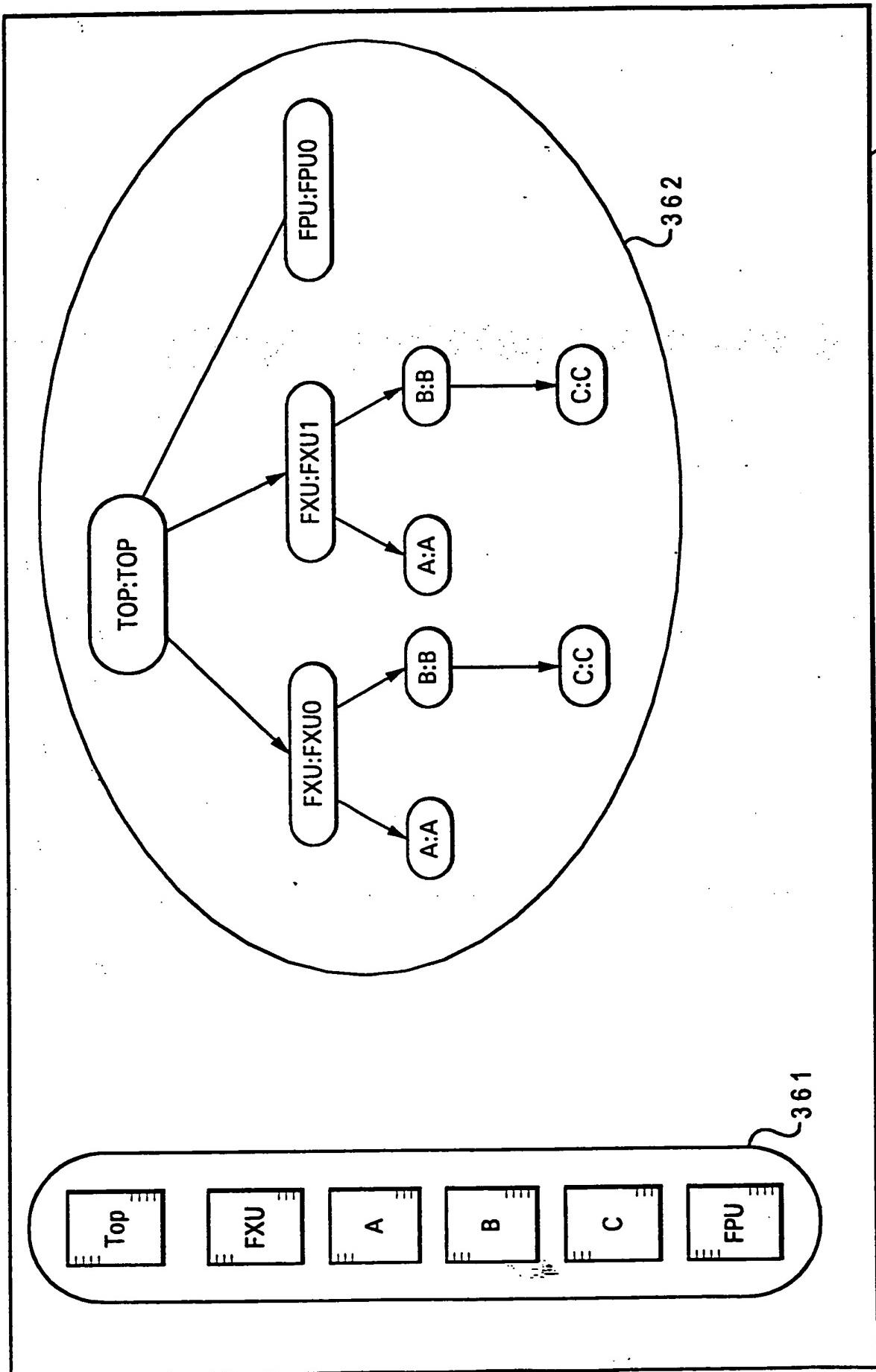


Fig. 3C

{ 44

Fig. 3D



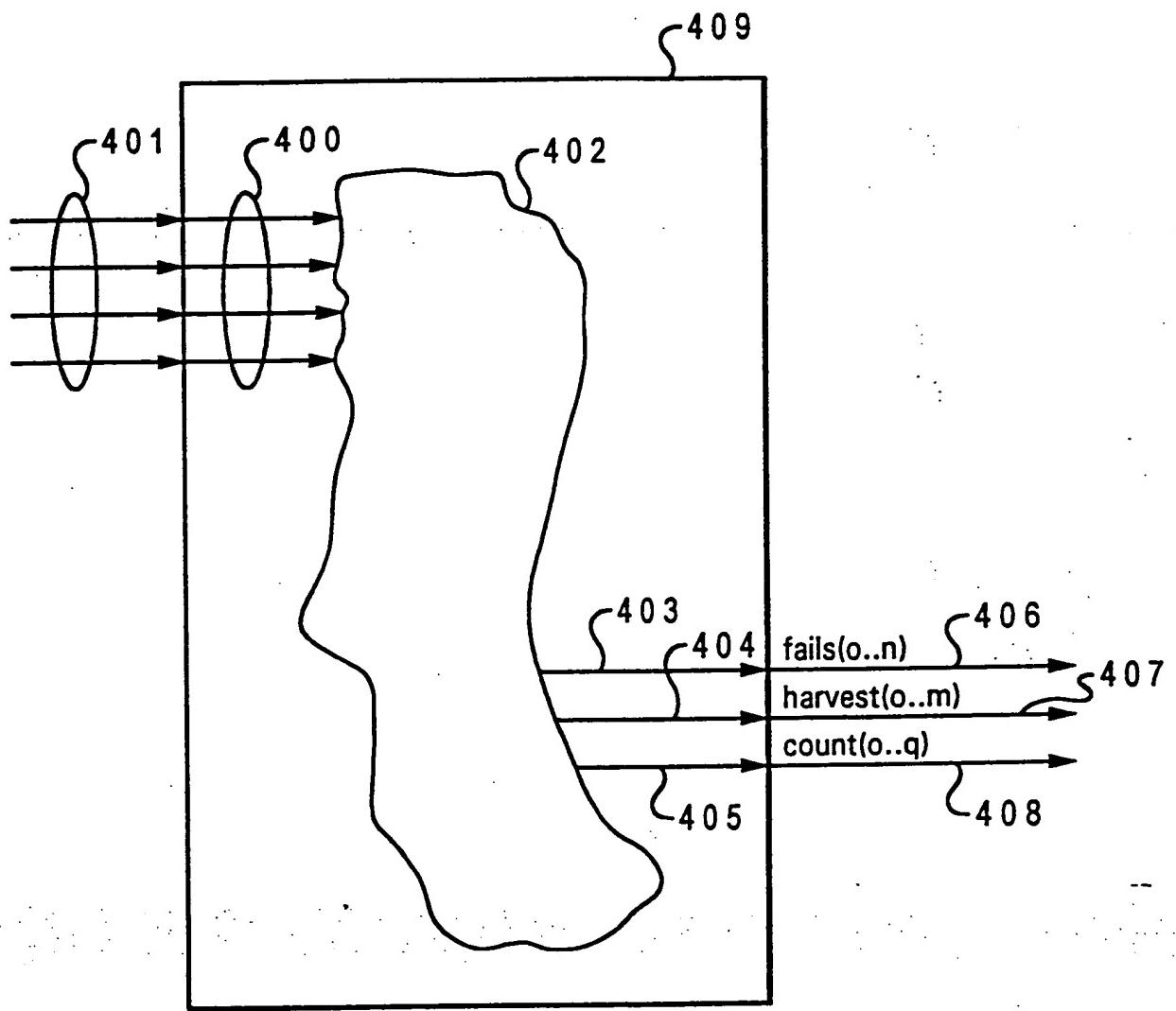


Fig. 4A

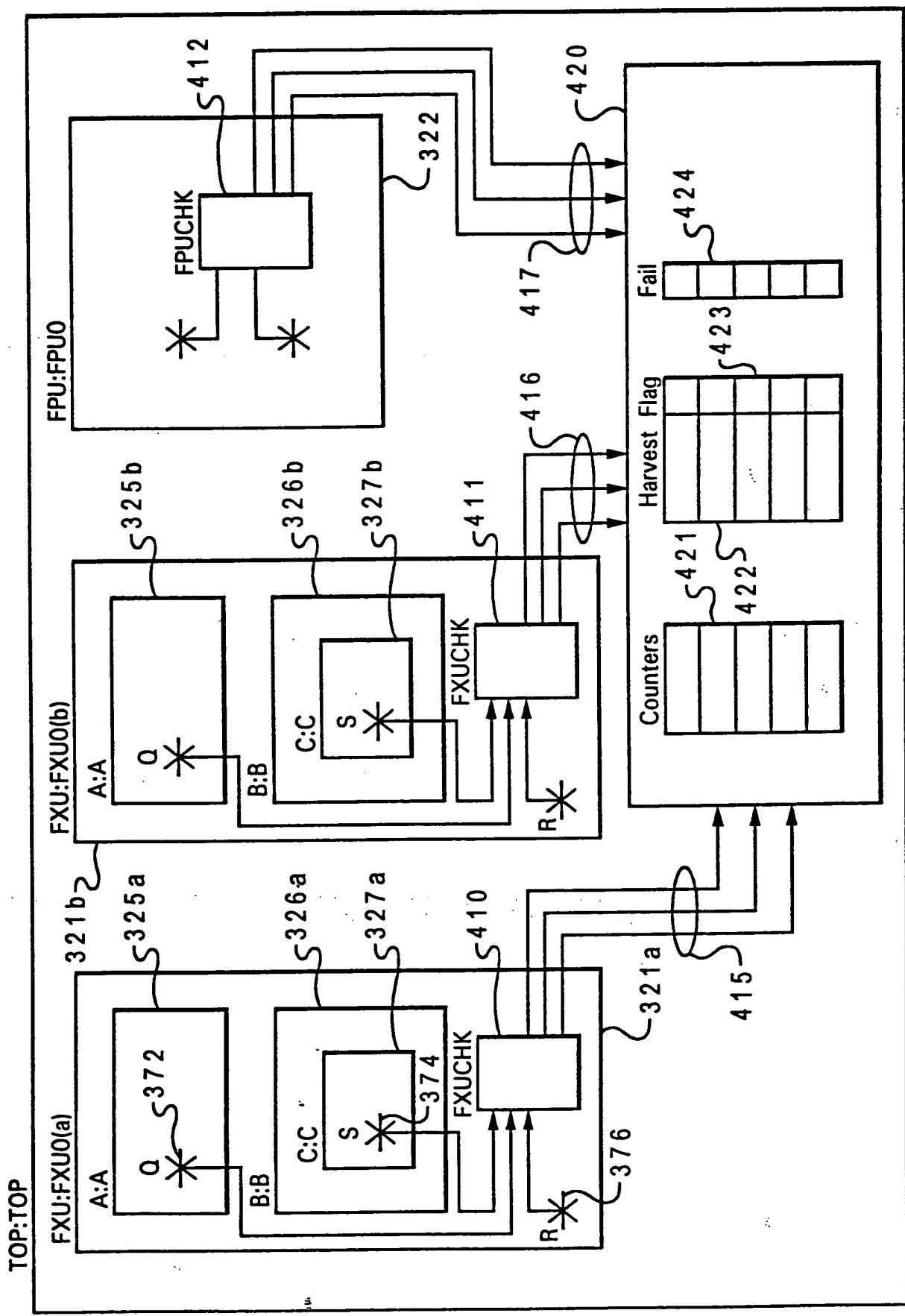


Fig. 4B

ENTITY FXUCHK IS

```
PORT( S_IN      : IN std_ulogic;
       Q_IN      : IN std_ulogic;
       R_IN      : IN std_ulogic;
       clock     : IN std_ulogic;
       fails     : OUT std_ulogic_vector(0 to 1);
       counts    : OUT std_ulogic_vector(0 to 2);
       harvests  : OUT std_ulogic_vector(0 to 1);
);
```

} 450

452 { -!! BEGIN
 -!! Design Entity: FXU;

453 { -!! Inputs
 -!! S_IN => B.C.S;
 -!! Q_IN => A.Q;
 -!! R_IN => R;
 -!! CLOCK => clock;
 -!! End Inputs

454 { -!! Fail Outputs;
 -!! 0 : "Fail message for failure event 0";
 -!! 1 : "Fail message for failure event 1";
 -!! End Fail Outputs;

455 { -!! Count Outputs;
 -!! 0 : <event0> clock;
 -!! 1 : <event1> clock;
 -!! 2 : <event2> clock;
 -!! End Count Outputs;

456 { -!! Harvest Outputs;
 -!! 0 : "Message for harvest event 0";
 -!! 1 : "Message for harvest event 1";
 -!! End Harvest Outputs;

457 { -!! End;

} 451

} 440

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

} 458

Fig. 4C

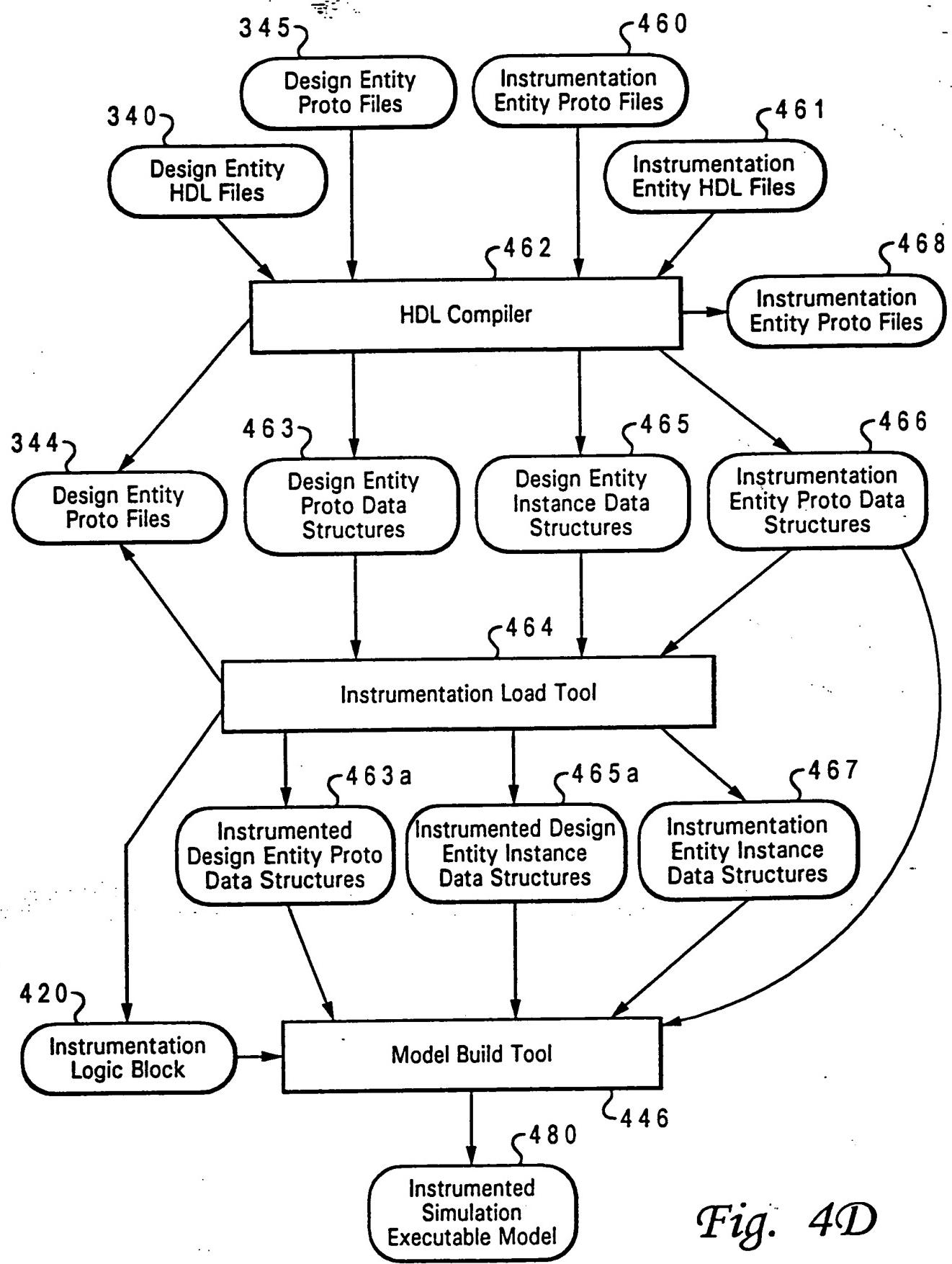
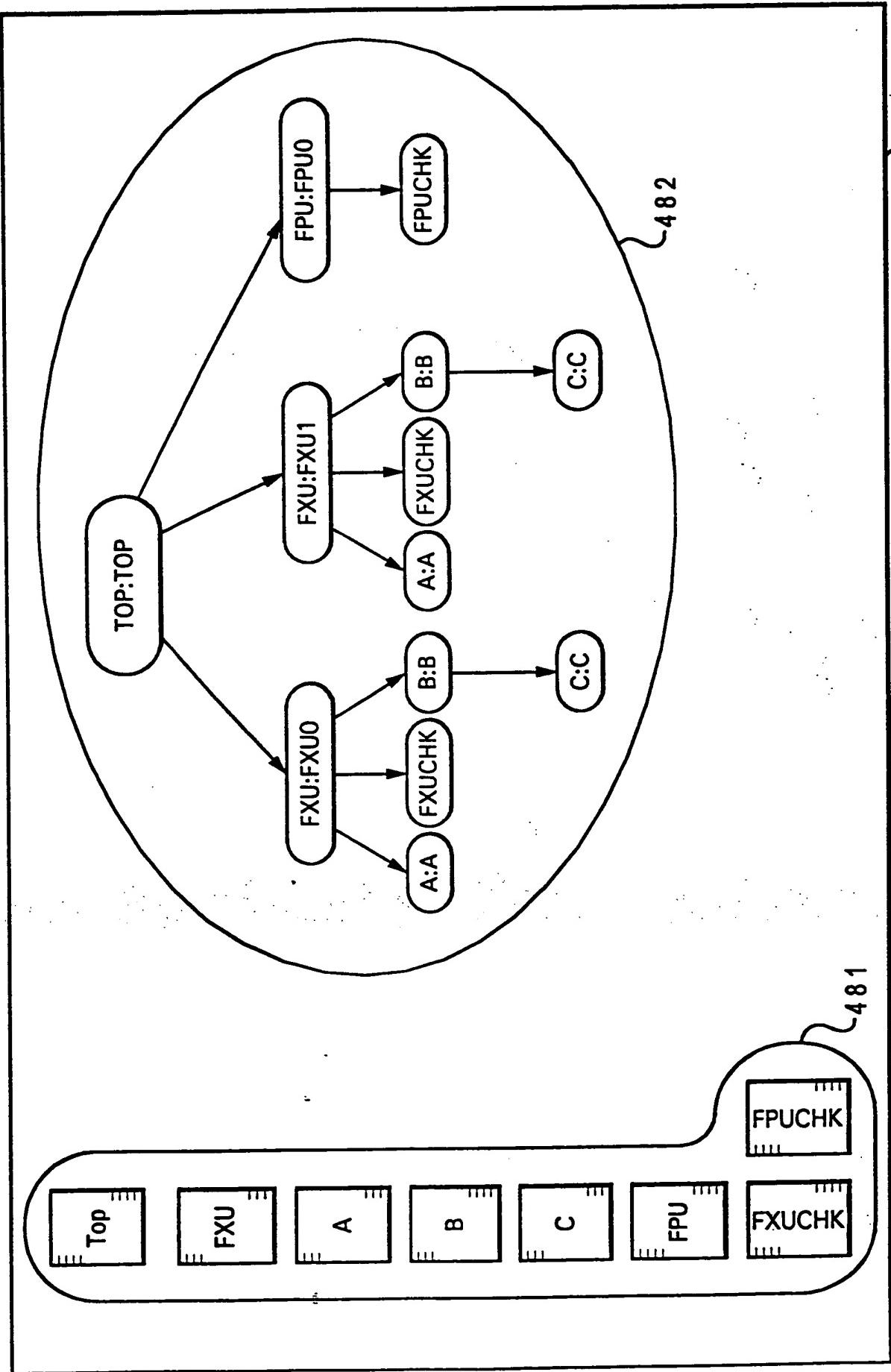
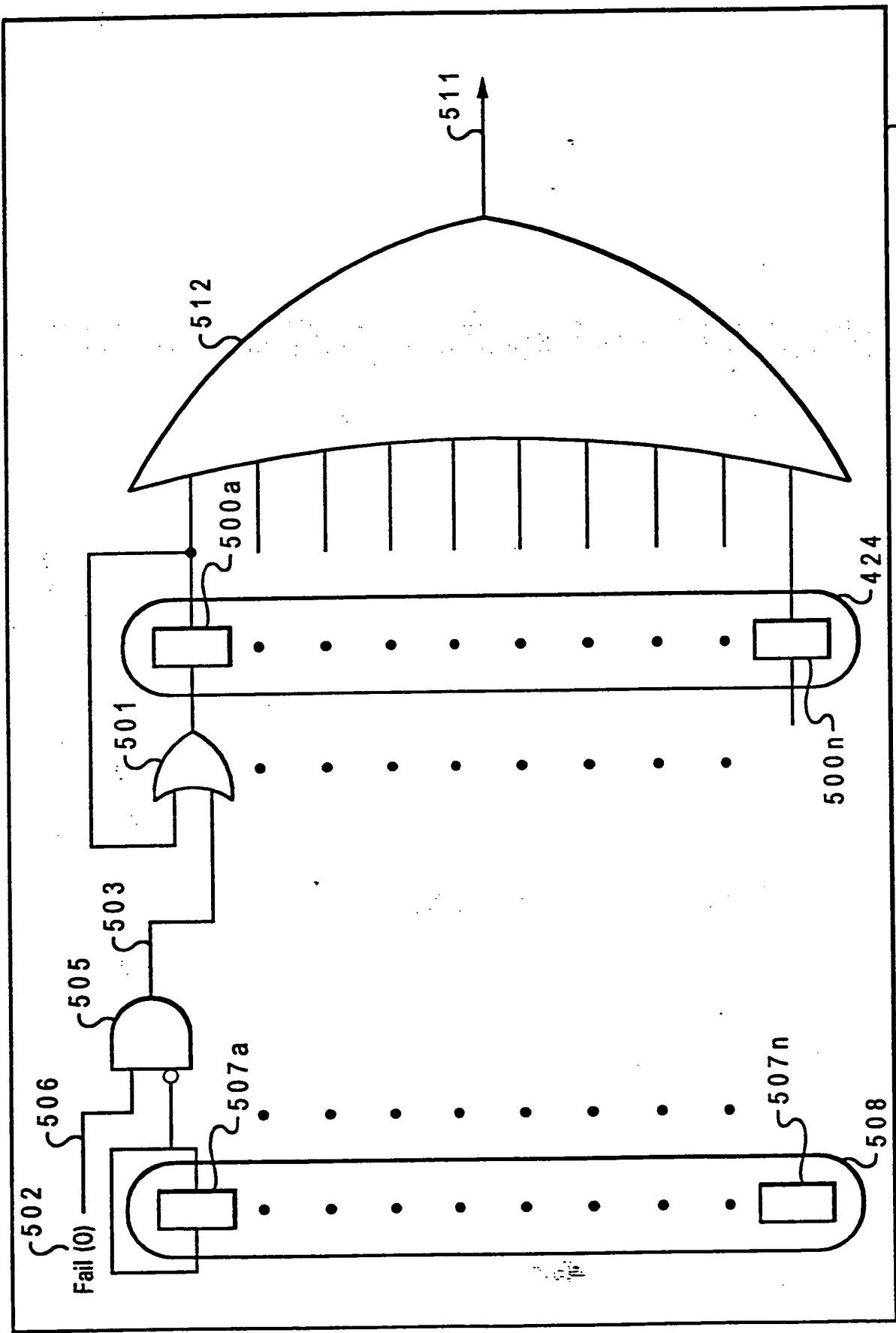


Fig. 4D

Fig. 4E



0000000000000000



{ 420

Fig. 5A

000000000000000000000000

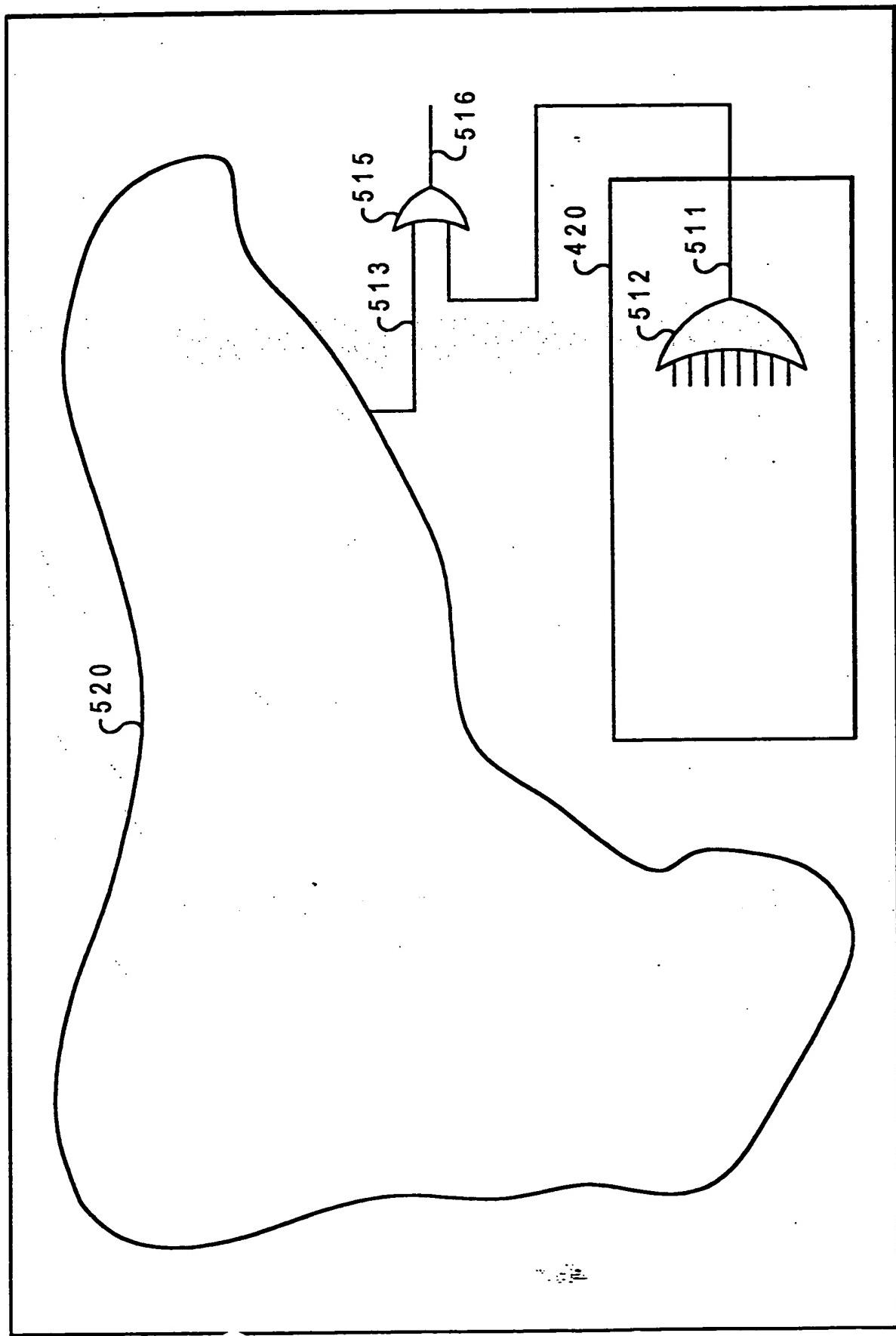
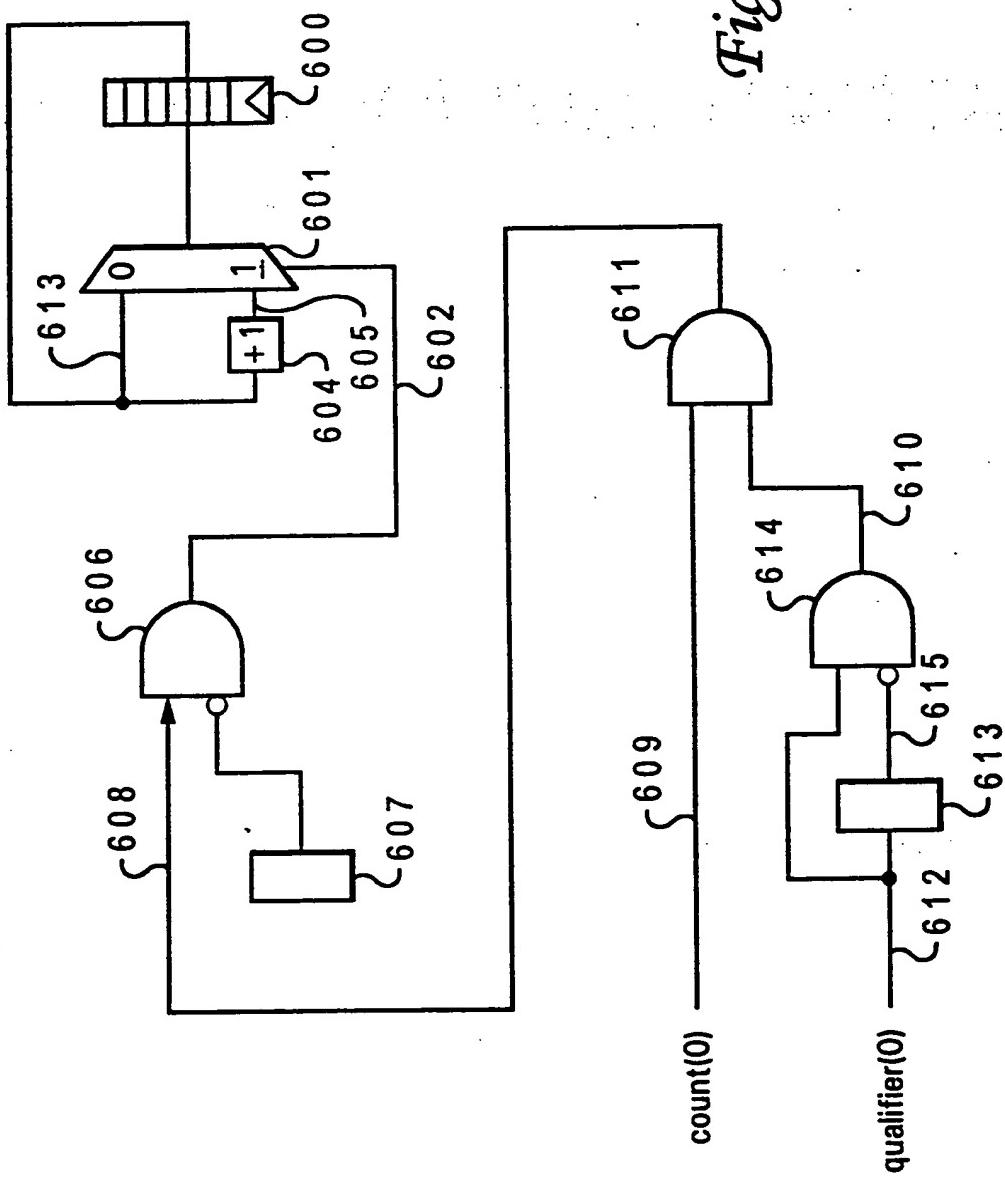


Fig. 5B

Fig. 6A



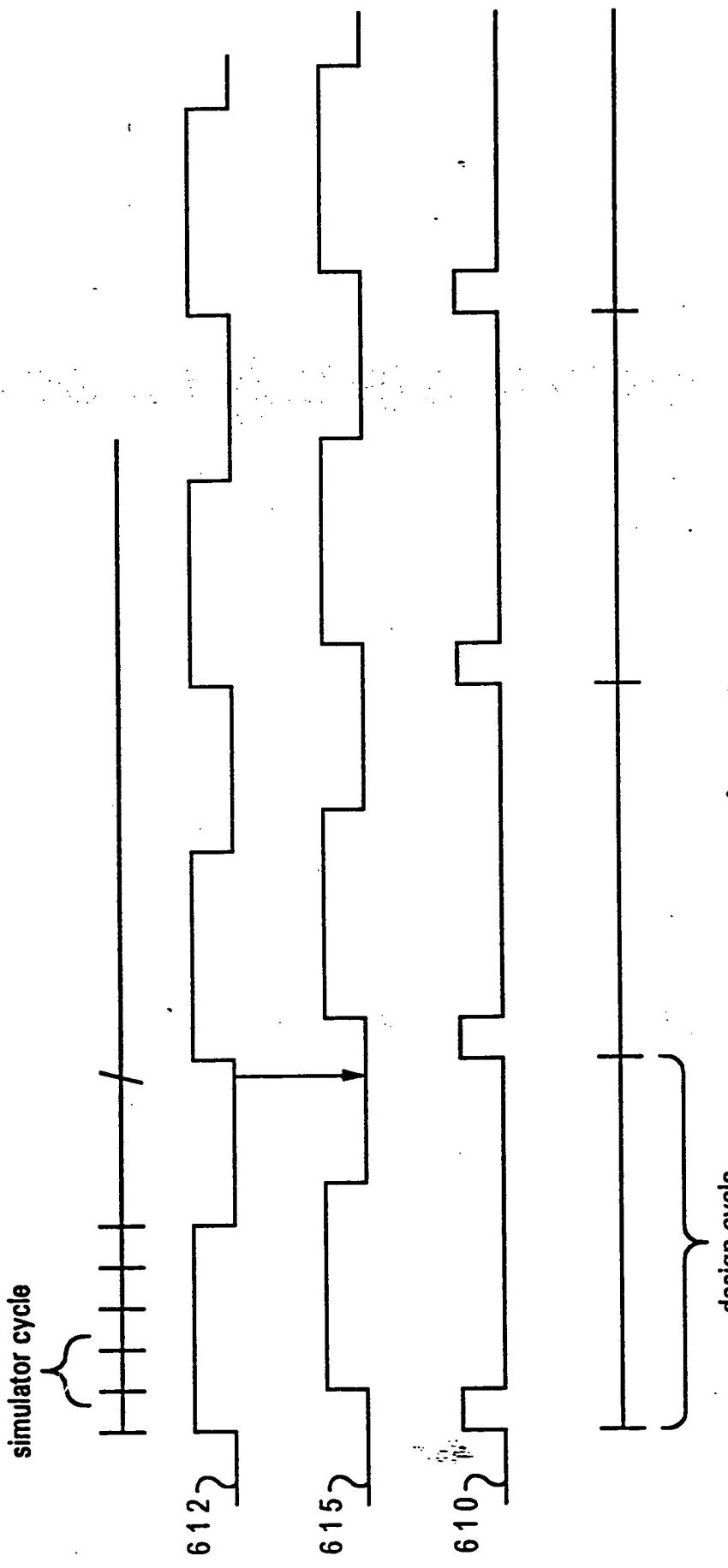


Fig. 6B

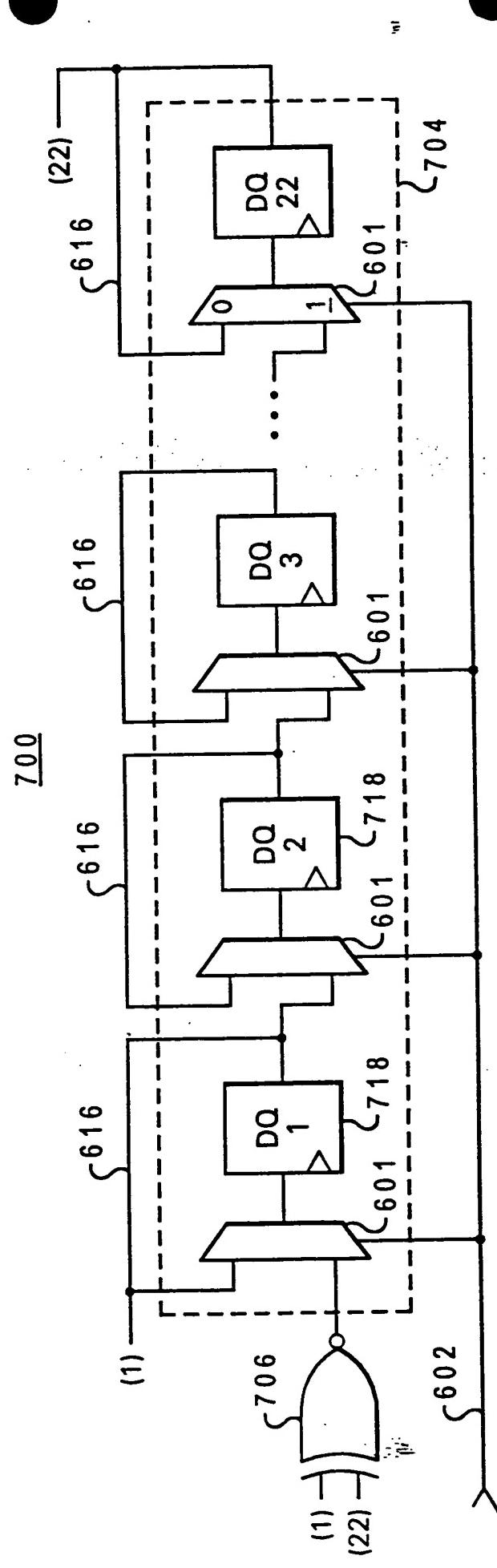


Fig. 7

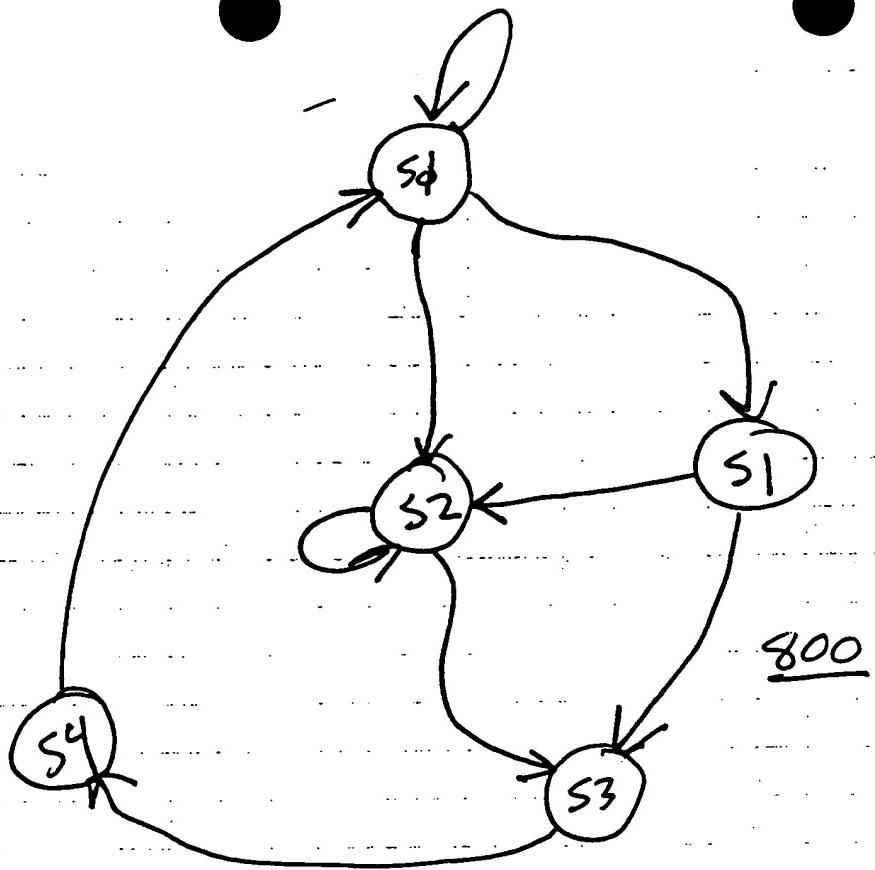


FIG. 8

(Prior Ant)

entity fsm; fsm

850

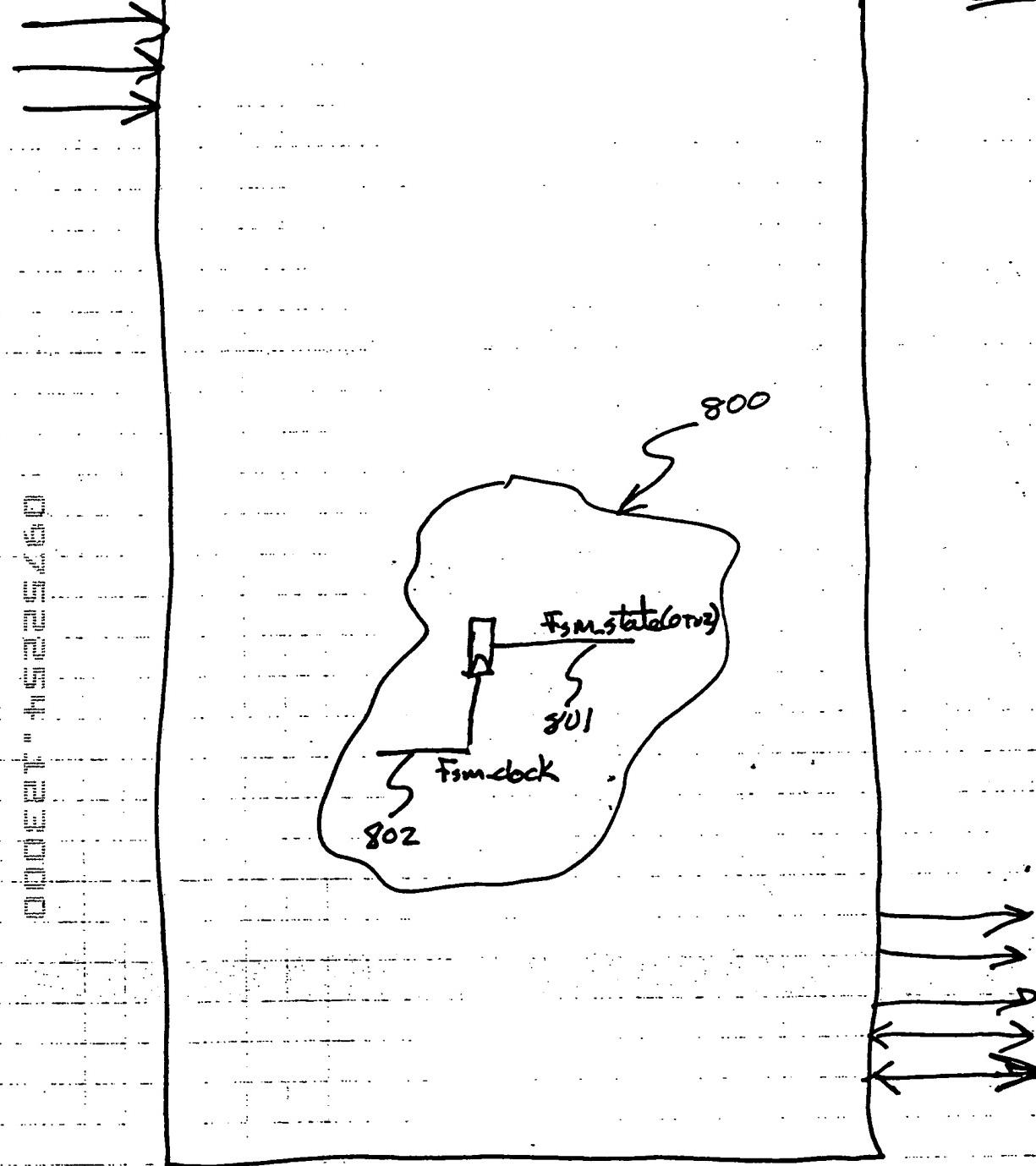


FIG. 8A
(Prior Art)

entity Fsm Is

PORT C

.... ports for entity fm... ..

3

Architecture fsm of fsm IS

BEGUN

.... HDL code for Fsm and rest of the entity.

fsm-state(0 to 2) <-- ... signal 801 ...

```

853 {
859 {
854 {
855 {
856 {
857 {
658 } }

--!! Embedded Fsm : exampleFsm;
--!! clock          : (fsm_clock);
--!! state_vector   : (fsm_state(0 to 2));
--!! states          : (s0, s1, s2, s3, s4);
--!! state_encoding  : ('000', '001', '010', '011', '100');
--!! arcs            : (s0 => s0, s0 => s1, s0 => s2,
--!!                      s1 => s2, s1 => s3, s2 => s2,
--!!                      s2 => s3, s3 => s4, s4 => s0);

--!! end Fsm;

```

END;

FIG. 8B

entity FSM:FSM



850

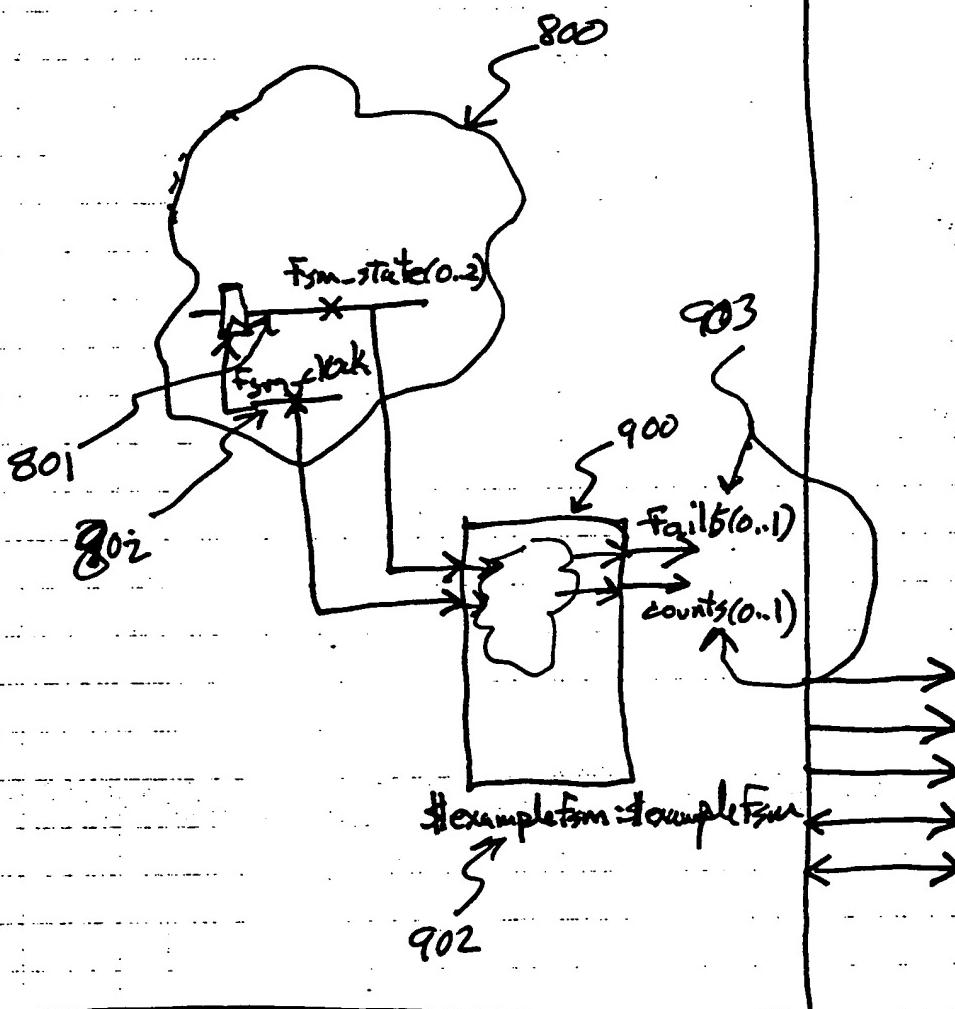


FIG. 9

TOP, TOP

X:111
Y:10a

83:83

1012a

81:81
1016a

82:82
1018a

X:112
Y:10b

83:83

1012b

z:z

81:81
1016b

82:82
1018b

z:z

X:111
Y:10c

84:84

1012c

81:81
1016c

82:82
1018c

z:z

FIG. 10A

10303

10323

10343

10363

<instantiation identifier>. <instrumentation entity name>. <design entity name>. <eventname>

1034

FIG 10B

1030

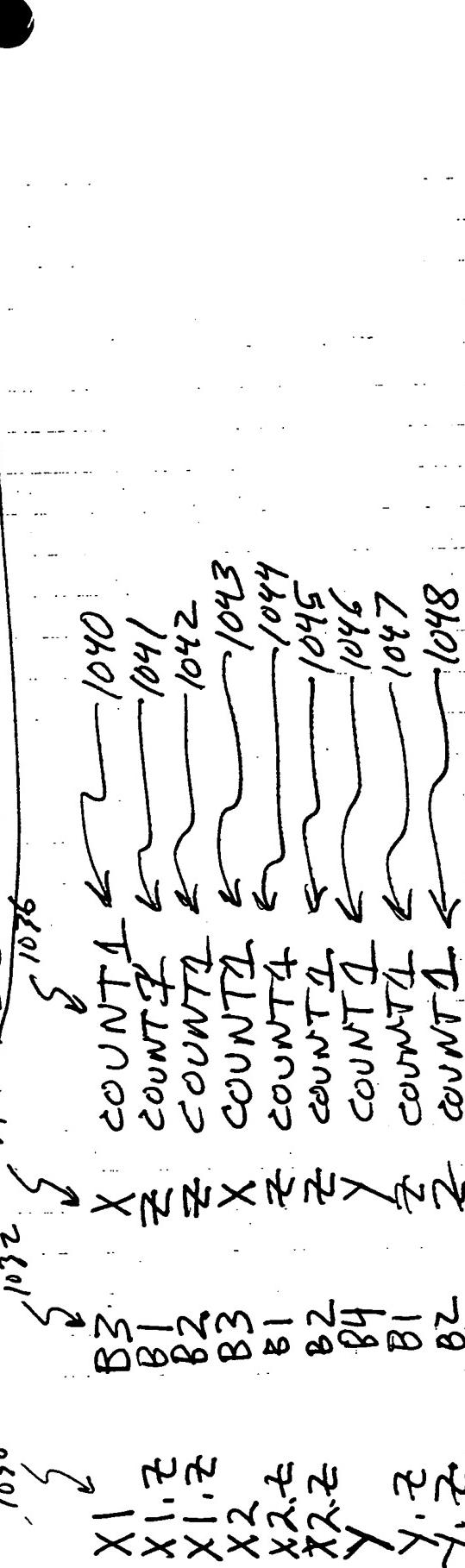


FIG 10C

1036

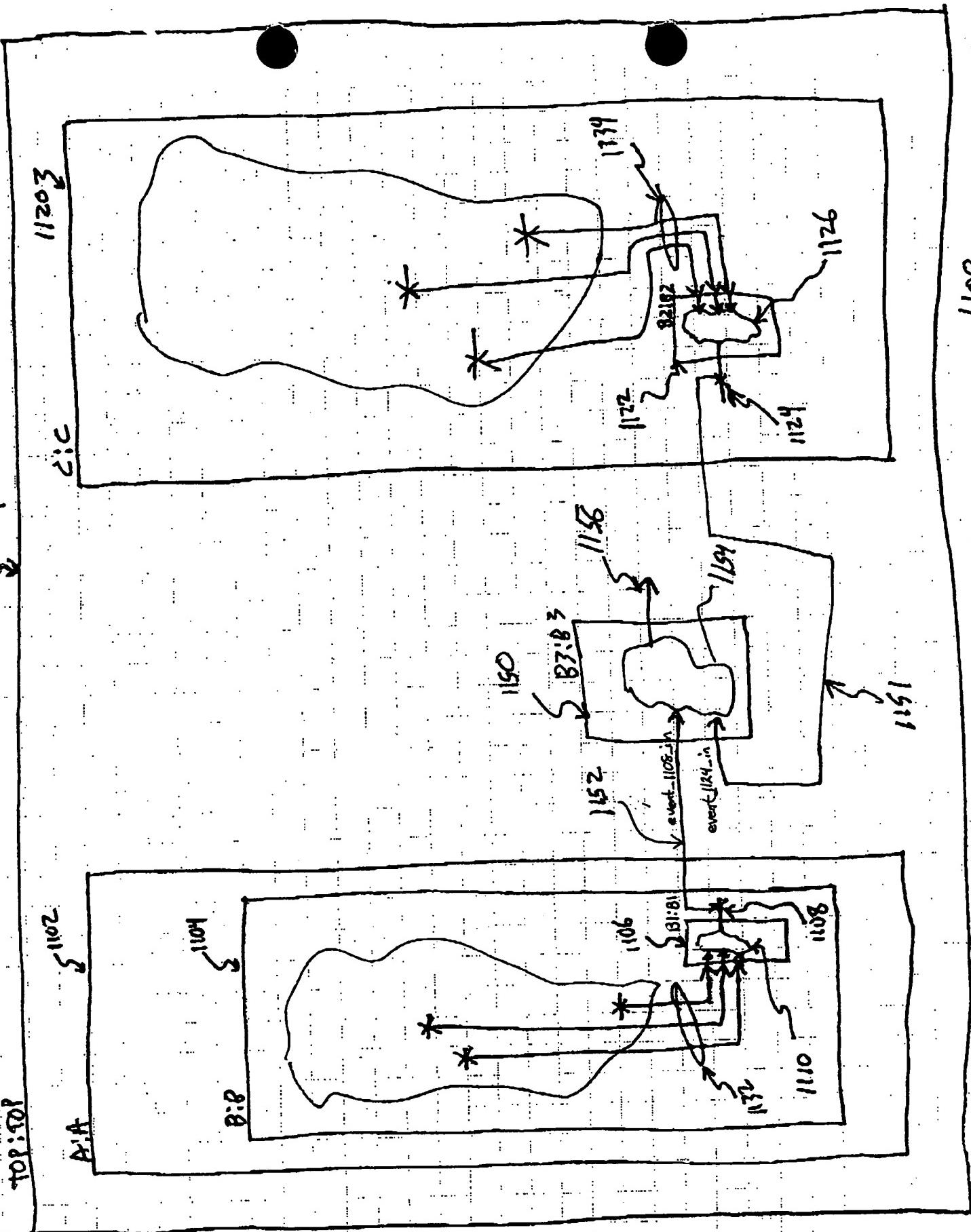
1034

1030

<instantiation identifier>. <design entity name>. <eventname>

FIG. 10D

BEST AVAILABLE COPY



BEST AVAILABLE COPY

```

--!! inputs          1165
--!! inputs          1163
--!! event_1108_in <= C.[B2.count.event_1108]; 3/1161
--!! event_1124_in <= A.B.[B1.count.event_1124]; 3/1162
--!! end inputs      1164

```

FIG. 118

```

--!! inputs          1166
--!! event_1108_in <= C.[count.event_1108]; 3/1171
--!! event_1124_in <= B.[count.event_1124]; 3/1172
--!! end inputs      1167

```

FIG. 11C